CLAIMS

What is claimed is:

1. A data transfer system comprising:

a plurality of data lines for transferring data signals and at least one control line for transferring a control signal, said plurality of data lines and said at least one control line being allocated in parallel;

a data driver connected to at least one of said plurality of data lines;

a control driver connected to at least one of said at least one control line; and

a host system, coupled to send and receive said data signals and said control signal to and from at least one storage device, setting a data signal slew rate and a control signal slew rate such that said data signal slew rate is smaller than said control signal slew rate.

2. The data transfer system according to claim 1, further comprising a table containing an optimum value of said control signal slew rate, said optimum value dependent on a quantity of devices connected to said host system, wherein said host system sets said optimum value of said control signal slew rate in said control driver upon said host system determining said quantity of devices.

3. The data transfer system according to claim 1, wherein said host system sets a data signal rising slew rate independently of a data signal falling slew rate, and said host sets a control signal rising slew rate independently of a control signal falling slew rate.

4. The data transfer system according to claim 1, wherein said control signal is a clock signal.

5. The data transfer system according to claim 1, wherein said data signals and said control signal conform to AT Attachment (ATA) Specifications.

6. The data transfer system according to claim 1, wherein said data signals and said control signal conform to ATA Packet Interface (ATAPI) Specifications.

7. The data transfer system according to claim 1, wherein a transition time of said data signal between a first reference data voltage and a second reference data voltage is longer than a transition time of said control signal between a first reference control voltage and a second reference control voltage by at least 2 nanoseconds.

8. A data transfer method for transferring, between a host system and a storage device, data signals via a plurality of data lines and a control signal via at least one control line, said plurality of data lines and said at least one control line being allocated in parallel, said method comprising the steps of:

setting a data signal slew rate smaller than a control signal slew rate;

generating via a plurality of drivers the data signals having said data signal slew rate and the control signal having said control signal slew rate; and

receiving said data signals and said control signal.

9. The data transfer method according to claim 8 further comprising the steps of:

determining a quantity of devices connected to a host system; and

setting an optimum value of said data signal slew rate and an optimum value of said control signal slew rate by referring to a table correlating said quantity of said connected devices to said optimum values of said data signal slew rates and said control signal slew rates.

10. The data transfer method according to claim 8, wherein a data signal rising slew rate is set independently of a data signal falling slew rate, and a control signal rising slew rate is set independently of a control signal falling slew rate.

11. The data transfer method according to claim 8, wherein said control signal is a clock signal.

12. The data transfer method according to claim 8, wherein said data signals and said control signal conform to AT Attachment (ATA) Specifications.

13. The data transfer method according to claim 8, wherein said data signals and said control signal conform to ATA Packet Interface (ATAPI) Specifications.

14. The data transfer method according to claim 8, wherein a transition time of said data signal between a first reference data voltage and a second reference data voltage is longer than a transition time of said control signal between a first reference control voltage and a second reference control voltage by at least 2 nanoseconds.

15. A storage device connected to a host system, said storage device comprising at least one driver in an interface section of said storage device, said at least one driver capable of transmitting to the host system multiple data signals via multiple data signal lines and at least one control signal via at least one control signal line, said multiple data signal lines and said at least one control signal line being allocated in parallel, and said at least one driver capable of sending said data signals with a variable data signal slew rate and said at least one control signal with a variable control signal slew rate, said data signal slew rate having been set smaller than said control signal slew rate by the host system.

16. The storage device according to claim 15, wherein said storage device, being one of at least one storage devices connected to the host system, further comprises a table correlating a quantity of said at least one storage devices to optimum values of said data signal slew rate and said control signal slew rate, and wherein said at least one driver transmits said multiple data signals and said at least one control signal at said optimum values.

17. The storage device according to claim 15, wherein said host system sets a data signal rising slew rate independently of a data signal falling slew rate, and a control signal rising slew rate independently of a control signal falling slew rate.

18. The storage device according to claim 15, wherein said control signal is a strobe signal conforming to AT Attachment (ATA) Specifications.

19. The storage device according to claim 15, wherein said control signal is a strobe signal conforming to ATA Packet Interface (ATAPI) Specifications.

20. The storage device according to claim 15, wherein a transition time of said data signal between a first reference data voltage and a second reference data voltage is longer than a transition time of said control signal between a first reference control voltage and a second reference control voltage by at least 2 nanoseconds.

21. A computer system comprising:

a host system;

a storage device;

a cable for connecting said host system interface and said storage device interface, said cable comprising multiple data signal lines and at least one control signal line allocated in parallel;

at least one driver in said host system and at least one driver in said storage device, each said at least one driver in said host system and each said at least one driver in said storage device being capable of generating a data signal and a control signal, each said data signal having a variable data signal slew rate and each said control signal having a variable control signal slew rate;

wherein said host system sets said variable data signal slew rate smaller than said variable control signal slew rate.

22. The computer system according to claim 21, said computer system further comprising a table containing an optimum value of said control signal slew rate corresponding to a quantity of devices connected to said host system, wherein said host system sets said optimum value of said control signal slew rate at said control driver upon said host system determining said quantity of devices.

23. The computer system according to claim 21, wherein said host system sets a data signal rising slew rate independently of a data signal falling slew rate, and said host system sets a control signal rising slew rate independently of a control signal falling slew rate.

24. The computer system according to claims 21, wherein said control signal is a strobe signal conforming to AT Attachment (ATA) Specifications;

25. The computer system according to claim 21, wherein said control signal is a strobe signal conforming to ATA Packet Interface (ATAPI) Specifications.

26. The computer system according to claim 21, wherein a transition time of said data signal between a first reference data voltage and a second reference data voltage is longer than a transition time of said control signal between a first reference control voltage and a second reference control voltage by at least 2 nanoseconds.